CLAIMS

1. A controlled switch comprising:

a control circuit for said switch, in a first phase said controlled circuit opens said controlled switch, in a second phase said control circuit closes said controlled switch; and

a MOS transistor having a source and a bulk, wherein in said first phase said bulk is electrically coupled to ground and in said second phase said bulk is electrically coupled to said source.

2. The controlled switch according to claim 1 wherein in said first phase a first control signal is present and in said second phase a second control signal is present.

3. The controlled switch according to claim 2 wherein in said first phase said bulk is coupled to ground by a switch controlled by said first control signal.

4. The controlled switch according to claim 2 wherein in said second phase said bulk is coupled to said source by a switch controlled by said second control signal.

5. The controlled switch according to claim 2 wherein said MOS transistor has the source connected to an input voltage and a drain connected to an output voltage, said control circuit comprises a first switch controlled by said second control signal, applied between said input voltage and a first terminal of a capacitor, a second switch controlled by said first control signal, applied between said first terminal of the capacitor and ground, a third switch controlled by a signal present on a gate of said MOS transistor, applied between a second terminal of said capacitor and a prefixed reference voltage, a fourth switch controlled by said second control signal, applied to

the second terminal of said capacitor and the gate of said MOS transistor, a fifth switch controlled by said first control signal, applied between the gate of said MOS transistor and ground.

6. A controlled switching circuit, comprising:

a first MOS transistor having source, drain, gate, and bulk terminals, the source and drain terminals being connected between an input and an output of the controlled switching circuit;

a first switch connected between the bulk terminal and a first reference voltage; and

a second switch connected between the bulk terminal and the input.

7. The controlled switching circuit of claim 6 wherein the second switch is connected between the source and bulk terminals.

8. The controlled switching circuit of claim 6 wherein the first switch is controlled by a first control signal and the second switch is controlled by a second control signal, the first and second control signals having non-overlapping active phases such that the second switch is open while the first switch is closed and the second switch is closed while the first switch is open.

9. The controlled switching circuit of claim 6 wherein the second switch includes complementary second and third MOS transistors connected in parallel between the bulk terminal of the first MOS transistor and the input, the second MOS transistor being controlled by a control signal and the third MOS transistor being controlled by an inverted form of the control signal.

10. The controlled switching circuit of claim 6, further comprising:

a capacitor having first and second terminals;

a third switch connected between the input and the first terminal of the capacitor;

a fourth switch connected between the second terminal of the capacitor and the gate terminal of the first MOS transistor; and

a fifth switch connected between the second terminal of the capacitor and a second reference voltage.

11. The controlled switching circuit of claim 10 wherein the fifth switch includes a control terminal connected to the gate of the first MOS transistor.

12. The controlled switching circuit of claim 10, further comprising:

a sixth switch connected between the first terminal of the capacitor and the first reference voltage, the fifth and sixth switches being controlled by a first control signal and the third and fourth switches being controlled by a second control signal, wherein the first and second control signals have non-overlapping active phases such that the third and fourth switches are open while the fifth and sixth switches are closed and the third and fourth switches are closed while the fifth and sixth switches are open.

13. The controlled switching circuit of claim 12, further comprising:

a seventh switch connected between the gate terminal of the first MOS transistor and the first reference voltage, the seventh switch having a control terminal connected to the first control signal such that the seventh switch is closed during the active phase of the first control signal, which connects a control terminal of the fifth switch to the first reference voltage and closes the fifth switch.

14. The controlled switching circuit of claim 10 wherein the fourth switch is an NMOS transistor having a bulk terminal and the fifth switch is a PMOS transistor with a bulk terminal connected to the bulk terminal of the fourth switch.

15. A method of controlling a MOS transistor having source, drain, gate, and bulk terminals, the method comprising:

opening the MOS transistor and connecting the bulk terminal to ground during a first phase; and

closing the MOS transistor and connecting the bulk terminal to one of the source and drain terminals during a second phase that does not overlap the first phase.

16. The method of claim 15 wherein the bulk and gate are respectively connected to ground by first and second switches and the bulk is connected to the one of the source and drain terminals by a third switch, the first and second switches being controlled by a first control signal and the third switch being controlled by a second control signal.

17. The method of claim 15, further comprising:

charging a capacitor to a reference voltage during the first phase; and

electrically connecting the capacitor to the gate terminal of the MOS transistor during the second phase.

18. The method of claim 17 wherein the charging step includes connecting a first terminal of the capacitor to ground and a second terminal of the capacitor to the reference voltage during the first phase and the electrically connecting step includes, during the second phase:

disconnecting the capacitor from ground and the reference voltage;

connecting the first terminal of the capacitor to an input voltage; and

connecting the second terminal of the capacitor to the gate terminal of the MOS transistor.

19. The method of claim 17 wherein the charging step includes connecting a first terminal of the capacitor to ground and a second terminal of the

capacitor to the reference voltage via a first switch during the first phase, the first switch having a control terminal connected to ground via a second switch connected between the gate terminal of the MOS transistor and ground.